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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,610	12/12/2003	Steven Frank	104853-0003	1959

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EXAMINER	
PRICE, NATHAN E	

ART UNIT	PAPER NUMBER
2194	

NOTIFICATION DATE	DELIVERY MODE
04/01/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@nutter.com

Office Action Summary	Application No.	Applicant(s)	
	10/735,610	FRANK ET AL.	
	Examiner	Art Unit	
	NATHAN PRICE	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 63 are pending. This Office Action is in response to communications received 05 January 2009. Previous objections and rejections not included in this Office Action have been withdrawn.

Response to Arguments

2. Applicant's arguments filed 05 January 2009 have been fully considered but they are not persuasive.

3. Applicant argues Sekiguchi fails to teach delivering an event to a thread by stating "...nowhere does Sekiguchi teach or suggest that the interrupt controller can deliver events to threads" (REMARKS, p. 17 ¶1).

4. However, Emer teaches treating each thread as executing on its own CPU (col. 1 lines 10 – 21). Therefore, when combined with the teaching of sending an interrupt to a specific CPU as taught by Sekiguchi (which is an interpretation Applicant appears to support by stating, "...that publication suggests that the controller can specify a CPU destination for an interrupt..." REMARKS, page 17 ¶1), the references teach or suggest sending an interrupt to a specific thread since Emer teaches treating each thread as executing on its own CPU. Therefore, although Sekiguchi focuses on delivering an

interrupt to a specific CPU, the combination of references teaches the interrupt is sent to the thread.

5. Additionally, Applicant argues Sekiguchi fails to teach event delivery without the processors executing instructions by stating "...processor instructions are actually required for interrupt delivery" (REMARKS, p. 17 ¶2). Applicant justifies this statement by describing the invocation of an interrupt handler.

6. However, the interrupt handler is called by the processor in response to the interrupt being received by the CPU. When the interrupt is received, the event has been delivered. Since the interrupt handler is executed after the event (interrupt) is delivered, the event delivery itself does not include execution of instructions by the processor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 -10, 13-19, 23-43, 46-49, 52-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer et al. (US 6,493,741 B1; "Emer") in view of Kelsey et al.

(US 7,082,519 B2; "Kelsey"), which incorporates by reference (col. 6 lines 58 – 64) Eggers (See reference "CA" on IDS submitted 12 December 2003), and Sekiguchi et al (US 2001/0016879 A1; "Sekiguchi").

8. As to claim 1, Emer teaches a processor, comprising

A. a plurality of processing units, each executing one or more processes or threads (which one or more processes or threads are collectively referred to as "threads") (col. 1 lines 10 – 21; col. 2 lines 16 – 21; col. 8 lines 1 – 7),

B. one or more execution units that are shared by, and in communication coupling with, the plurality of processing units, the execution units executing instructions from the threads (col. 1 lines 10 – 21; col. 2 lines 16 – 21; col. 8 lines 1 – 7),

C. an event delivery mechanism that delivers events to respective threads with which those events are associated, wherein the event delivery mechanism is in communication coupling with the plurality of processing units (col. 1 lines 10 – 21; col. 2 lines 16 – 21; col. 3 lines 25 – 28; col. 8 lines 1 – 7).

9. Emer fails to specifically teach the processor is an embedded processor and the event delivery mechanism delivers each such event to the respective thread without execution of instructions by said processing units. However, Kelsey teaches the

processor is an embedded processor and an event delivery mechanism that delivers events to respective threads with which those events are associated (col. 4 lines 11 – 19; col. 8 lines 60 – 67). It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Kelsey teaches additional features and characteristics of processors similar to the simultaneous multithreaded processors taught by Emer.

10. Furthermore, Sekiguchi teaches an event delivery mechanism that delivers events to respective threads with which those events are associated, wherein the event delivery mechanism delivers each such event to the respective thread without execution of instructions by said processing units (¶226, 228 and 231). It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Sekiguchi teaches an interrupt delivery system usable with the processors taught by both Emer and Kelsey.

11. As to claim 2, Emer teaches the thread to which an event is delivered processes that event without execution of instructions outside that thread (col. 6 lines 1 – 11).

12. As to claim 3, Emer teaches the events include any of hardware interrupts, software-initiated signaling events ("software events") and memory events (col. 3 lines 36 – 41).

13. As to claim 4, Eggers teaches the execution units execute instructions from the threads without need to know what thread they are from (p. 13 right column ¶3).

14. As to claim 5, Emer teaches each thread is any of constrained or not constrained to execute on a same processing unit during a life of that thread (col. 9 lines 5 – 7).

15. As to claim 6, Emer teaches at least one of the processing units is a virtual processing unit (col. 1 lines 10 – 21).

16. As to claim 7, Kelsey teaches a plurality of execution units and a pipeline control that is in communication coupling with the plurality of processing units and with the plurality of execution units, the pipeline control launching instructions from plural ones of the threads for concurrent execution on plural ones of the execution units (col. 12 lines 29 – 40). See the rejection of claims 1 – 3, 5 and 6 regarding limitations not specifically addressed in this rejection.

17. As to claim 8, Emer teaches the pipeline control comprises a plurality of instruction queues, each associated with a respective virtual processing unit (col. 4 lines 15 – 24).

18. As to claim 9, Kelsey teaches the pipeline control decodes instruction classes from the instruction queues (col. 12 lines 29 – 40).

19. As to claim 10, Kelsey teaches the pipeline control controls access by the processing units to a resource providing source and destination registers for the instructions dispatched from the instruction queues (col. 11 lines 40 – 48).

20. As to claim 13, Kelsey teaches the pipeline control controls access by the virtual processing units to the execution units (col. 12 lines 29 – 40).

21. As to claim 14, Emer teaches the pipeline control signals a branch execution unit that is shared by the virtual processing unit as the instruction queue for each virtual processing unit is emptied (col. 13 line 55).

22. As to claim 15, Emer teaches the pipeline control idles the execution units to decrease power consumption (col. 4 lines 32 – 34).

23. As to claim 16, Emer teaches the plurality of execution units include any of integer, floating, branch, compare and memory units (col. 13 line 55).

24. As to claim 17, see the rejection of claims 1, 5, 6, 7 and 16.

25. As to claims 18 and 19, see the rejection of claims 2 and 3.

26. As to claim 23, see the rejection of claims 7 and 8.

27. As to claim 24, Eggers teaches one or more instructions are fetched at a time for a said thread with a goal of keeping the instructions queues at equal levels (p. 14 right column ¶ 3 – 4).

28. As to claim 25, Kelsey teaches the pipeline control dispatches one or more instructions at a time from a given instruction queue for execution (col. 12 lines 29 – 40).

29. As to claim 27, see the rejection of claim 7.

30. As to claim 28, see the rejection of claims 1 and 5.

31. As to claims 29 – 31, see the rejection of claims 2, 3 and 6.

32. As to claims 32 – 34, see the rejection of claims 17, 2 and 3.

33. As to claims 35 – 40, see the rejection of claims 1 – 6.

34. As to claim 41, see the rejection of claims 1 – 3, 5 and 6.

35. As to claims 42, 43 and 46, see the rejection of claims 9, 10 and 16.

36. As to claims 47 – 49, 52 – 54 and 56, see the rejection of claims 17, 2, 3, 7, 8, 24 and 25.

37. As to claim 57, see the rejection of claims 1 and 5.

38. As to claims 58 – 60, see the rejection of claims 2, 3 and 6.

39. As to claims 61 – 63, see the rejection of claims 17, 2 and 3.

40. Claims 11, 12, 20 – 22, 44, 45, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer in view of Kelsey, which incorporates by reference Eggers, and Sekiguchi as applied to claims 8, 18, 41 and 48 above, and further in view of Microsoft Computer Dictionary (see PTO-892 mailed with this Office Action).

41. As to claims 11 and 12, Emer fails to specifically teach branch execution units as claimed. However, Emer does teach performing branch operations (col. 13 line 55) and branch units are well known, for example, see the definition of "branch instruction", "branchpoint" and "branch prediction" in Microsoft Computer Dictionary. Therefore, it would have been obvious to one of ordinary skill in the art to have (claim 11) the execution units include a branch execution unit responsible for any of instruction

address generation, address translation and instruction fetching and (claim 12) the branch execution unit maintains state for the virtual processing units.

42. As to claims 20, 21, 50 and 51, see the rejection of claim 11.

43. As to claim 22, see the rejection of claim 12.

44. As to claims 44 and 45, see the rejection of claims 11 and 12.

45. Claims 26 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer in view of Kelsey, which incorporates by reference Eggers, and Sekiguchi as applied to claims 25 and 54 above, and further in view of Blandy (US 6,912,647 B1).

46. As to claim 26, Emer fails to specifically teach stop flags as claimed. However, Blandy teaches a number of instructions dispatched by the pipeline control at a given time from a given instruction queue is controlled by a stop flag in a sequence of instructions in that queue (col. 5 lines 24 – 44). It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Blandy teaches how to further improve the performance of the processors disclosed by Emer by controlling execution in parallel systems.

47. As to claim 55, see the rejection of claim 26.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NATHAN PRICE whose telephone number is (571)272-4196. The examiner can normally be reached on 8:30am - 5:00pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NP

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192